

Short Course Name:

RTL Design, Verification, Synthesis and PnR for Digital VLSI Design

Instructors:

1. **Dr. Shahriyar Masud Rizvi**

*Deputy Director, Center for VLSI & Embedded Systems (CVES)*

*Dr. Anwarul Abedin Institute of Innovation*

*Associate Professor, Department of Electrical and Electronics Engineering (EEE)*

*American International University-Bangladesh (AIUB)*

*16+ years' experience in teaching RTL design (SystemVerilog/VHDL) and VLSI design*

2. **Mr. Ataus Shafi**

*Physical Design Engineer with extensive experience in the semiconductor industry, including at Ulkasemi and DSi*



**Prerequisites**

An undergraduate degree in Electrical and Electronic Engineering/Computer Engineering/Electrical Engineering or in a related field.  
Adequate knowledge of digital logic design, including timing/operation of sequential logic.

OR

Completion of at least one course in VLSI design—applicable for AIUB students who are pursuing an undergraduate degree in Electrical and Electronic Engineering/Computer Engineering/Computer Science & Engineering.

Knowledge of Verilog HDL or VHDL is preferred but not required.

**Course length and timings**

Course	Lecture and lab hours/week	Total lecture and lab hours	No. of weeks
RTL Design, Verification, Synthesis and PnR for Digital VLSI Design	5	50	10 + 1 (10 weeks of class and 1 week of evaluation)

**Highlights:**

Topic	EDA Tool
RTL Design with SystemVerilog	Xcelium (Cadence)
Functional Verification	Xcelium, vManager (Cadence)
Logic Synthesis	Genus (Cadence)
Place and Route (PnR)	Innovus (Cadence)

**Lecture Plan:**

Week	Class	Date	Day	Time	Content
1	1	24/01/26	Saturday	09:30am—02:30pm	<ul style="list-style-type: none"> <li>• Introduction to putty, tmux, vi and GitHub,</li> </ul>
					<ul style="list-style-type: none"> <li>• Review of <ul style="list-style-type: none"> <li>○ Basic digital logic,</li> <li>○ FPGA and ASIC architectures,</li> <li>○ Design flows for ASICs,</li> <li>○ Different views of standard cells (RTL, schematic and layout)</li> <li>○ Introduction to SystemVerilog HDL</li> </ul> </li> </ul>
2	2	31/01/26	Saturday	09:30am—02:30pm	<ul style="list-style-type: none"> <li>• Combinational logic design (e.g., datapath elements) with SystemVerilog</li> <li>• Linear Testbench design with SystemVerilog</li> </ul>
					<ul style="list-style-type: none"> <li>• Combinational logic design and Linear Testbench (continued)</li> </ul>
3	3	07/02/26	Saturday	09:30am—02:30pm	<ul style="list-style-type: none"> <li>• Design structuring</li> </ul>
					<ul style="list-style-type: none"> <li>• <b>Project submission on combinational logic design with SystemVerilog</b></li> </ul>
4	4	14/02/26	Saturday	09:30am—02:30pm	<ul style="list-style-type: none"> <li>• Sequential logic and memory design with SystemVerilog</li> </ul>
					<ul style="list-style-type: none"> <li>• Introduction to Finite State Machine (FSM) design with SystemVerilog</li> <li>• Digital System Design with FSMs.</li> </ul>
5	5	28/02/26	Saturday	09:30am—02:30pm	<ul style="list-style-type: none"> <li>• Digital System Design with FSMs (continued)</li> </ul>
					<ul style="list-style-type: none"> <li>• Advanced SystemVerilog design features.</li> <li>• SystemVerilog scheduling semantics, race conditions</li> <li>• Class-based testbench architecture design with SystemVerilog</li> <li>• Transactions, randomization and virtual interface</li> </ul>
6	6	07/03/26	Saturday	09:30am—02:30pm	<ul style="list-style-type: none"> <li>• Constrained random verification (CRV)</li> <li>• Functional coverage</li> <li>• Logic Synthesis for ASICs</li> </ul>
					<ul style="list-style-type: none"> <li>• Logic Synthesis for ASICs (continued)</li> <li>• Specifying timing constraints for ASICs</li> <li>• Design for Power, Performance and Area (PPA)</li> </ul>
7	7	14/03/26	Saturday	09:30am—02:30pm	<ul style="list-style-type: none"> <li>• <b>Project submission on digital system design with SystemVerilog</b></li> </ul>
					<ul style="list-style-type: none"> <li>• Floorplanning, Place and Route (PnR) and full-chip layout (RTL to GDS II) for ASICs</li> <li>• Static Timing Analysis</li> </ul>
8	8	21/03/26	Saturday	09:30am—02:30pm	<ul style="list-style-type: none"> <li>• Floorplanning and PnR (Continued) and sign-off</li> </ul>
					<ul style="list-style-type: none"> <li>• Floorplanning and PnR (Continued) and sign-off</li> </ul>
9	9	28/03/26	Saturday	09:30am—02:30pm	<ul style="list-style-type: none"> <li>• RISC architecture.</li> <li>• SystemVerilog RTL development for a RISC processor</li> </ul>
					<ul style="list-style-type: none"> <li>• Logic Synthesis and PnR for a RISC processor.</li> </ul>
10	10	04/04/26	Saturday	09:30am—02:30pm	<ul style="list-style-type: none"> <li>• Discussions on Final Project</li> </ul>
					<ul style="list-style-type: none"> <li>• Discussions on Final Project</li> </ul>
11					<ul style="list-style-type: none"> <li>• <b>Final Project submission on design, verification, synthesis and PnR of a complex digital system</b></li> </ul>